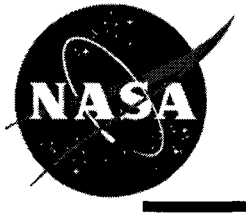
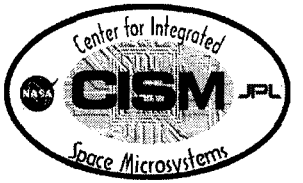
CL01-0562

FINAL



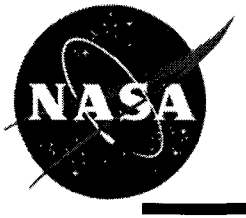


NASA's System on a Chip Technology Program

Mohammad M. Mojarradi
Center for Integrated Space Microsystems
Jet Propulsion Laboratory,
California Institute of Technology

URL: http://cism.jpl.nasa.gov

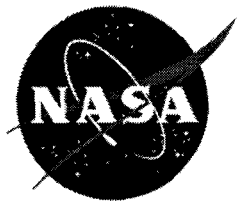
JPL



Outline

- Review of the JPL/CISM program goals
- Review of the SOAC program objectives
- Discuss SOAC technology directions

  Integration technology
  Power management
  Sensors
  On-chip power sources
- Overview of the Revolutionary Computing
- Summary



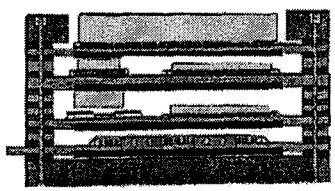
Center for Integrated Space Microsystems

CISM:

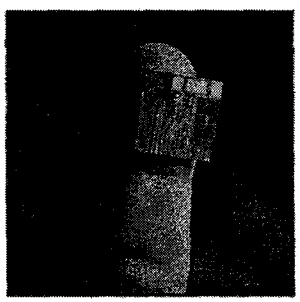
- Is a JPL Center of Excellence (COE)
  (JPL is a NASA COE in Deep-Space Exploration)
- Is an element of NASA's Deep Space Systems Development Program (X2000)
- Main focus is the advanced technology development of integrated avionics systems, system on a chip technologies, and revolutionary computing technologies.

Long-Term Focus on Future Deep-Space Exploration

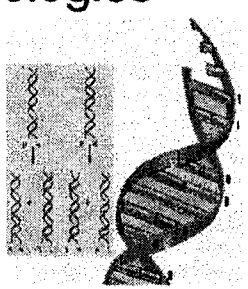
- Advanced Integrated Microelectronics



- Avionics Systems On A Chip



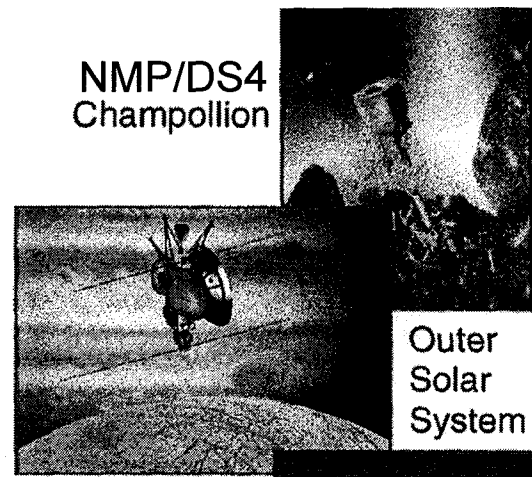
- Revolutionary Computing Technologies



Enabling Revolutionary Space Science

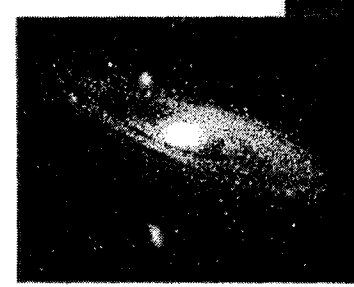
CISM will develop cross-cutting microelectronics and micro-avionics technologies and systems

NMP/DS4
Champollion



Outer Solar System

Mars Sample Return

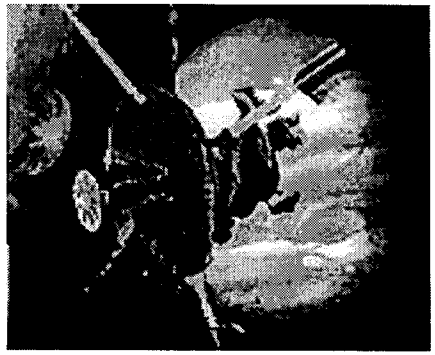


Interstellar Probe

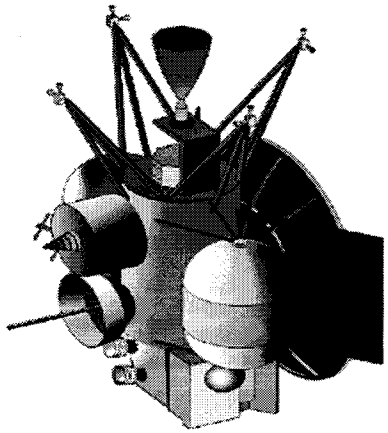
...and other future missions

Vision:
Towards a '*Thinking Evolvable*' Spacecraft

"Galileo"

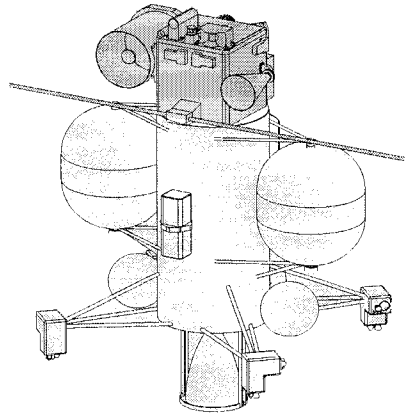


Fixed HW Design
Fixed SW Design



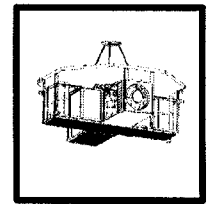
Fixed HW Design
Upgradable SW

"X2000"



Reconfigurable HW
Upgradable SW

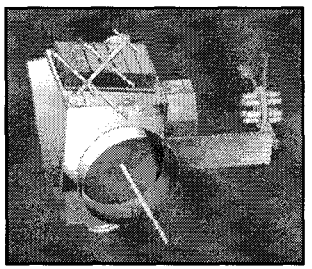
"Thinking S/C"



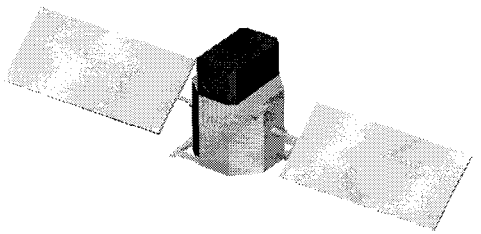
Evolvable HW
Upgradable SW
Autonomous Navigation,
Intelligent Systems

80's State of Art 2006 2020

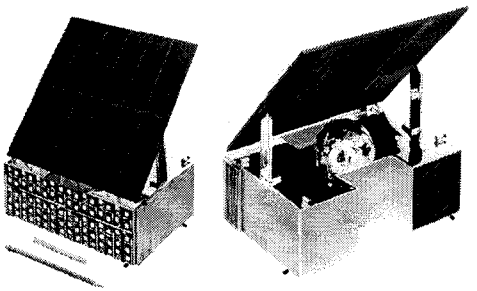
X2000 Strategy: Deliver New Generation of Spacecraft Systems every 3 years



X2000 1st Delivery
(YR 2000)



X2000 2nd Delivery
(YR 2003)

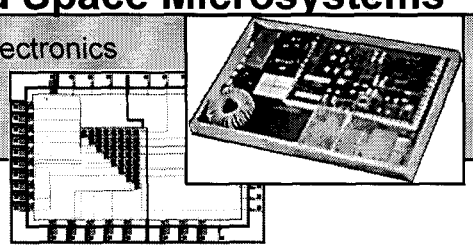


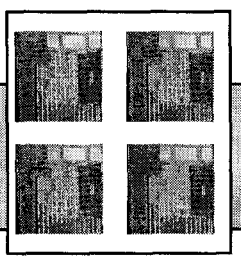
X2000 3rd Delivery
(YR 2006)

Technology Focus:

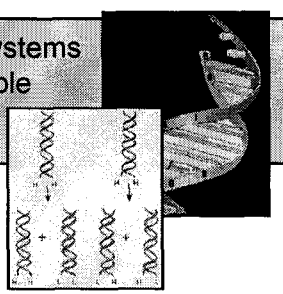
Integrated Space Microsystems

Low-Power Electronics
Autonomy
Data Systems





Evolvable Systems
Reconfigurable
Hardware

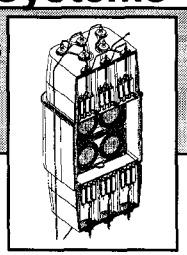


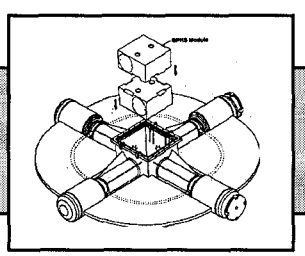
Novel
Computing
Concepts

Technology Focus:

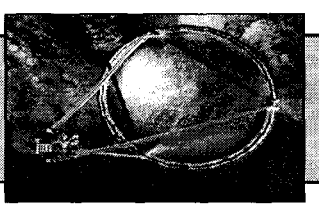
Advanced Power Systems

High-Efficiency Converters
"Bulletproof" Design
New Heat Source



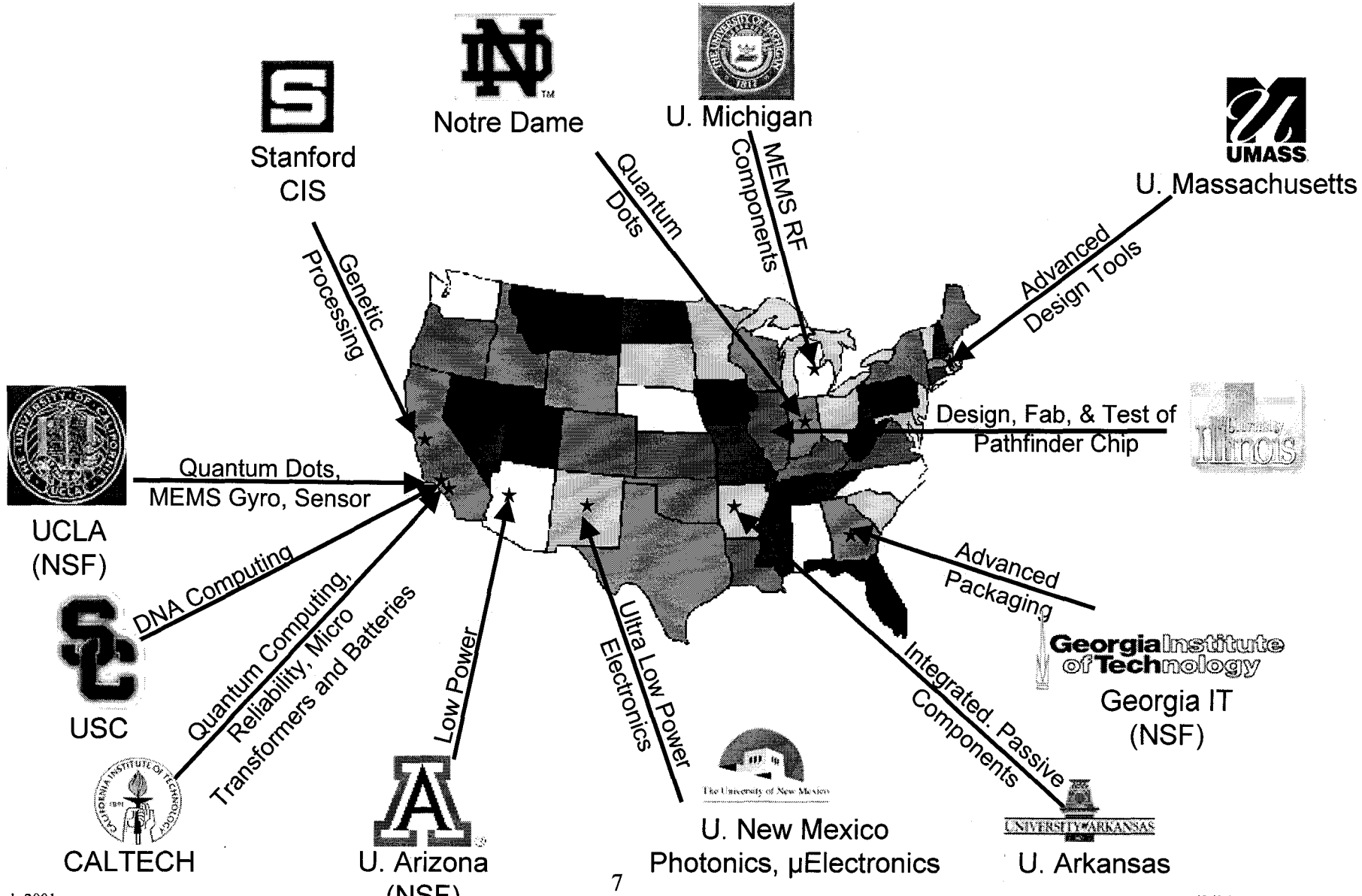


Miniature Generators

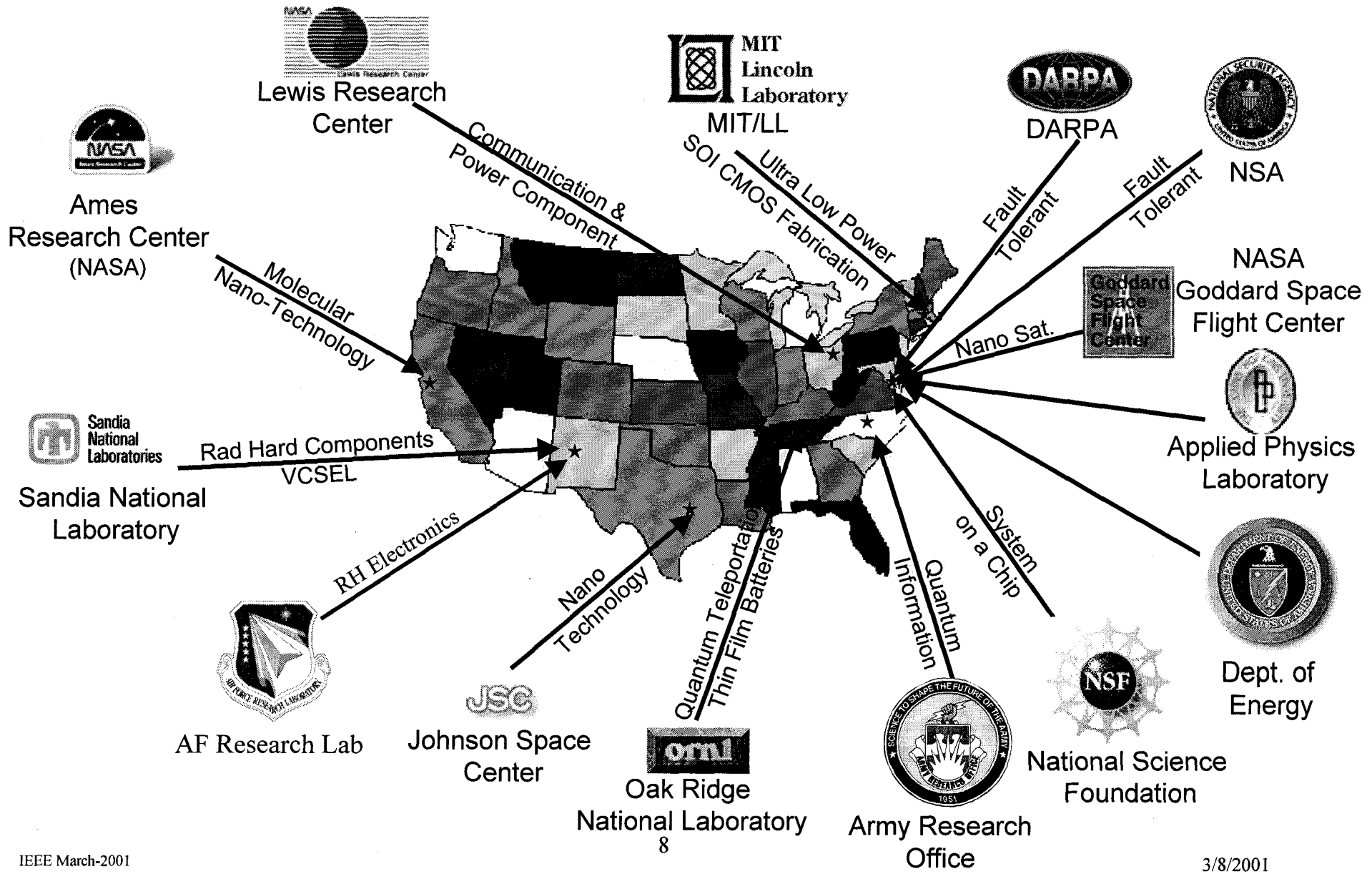


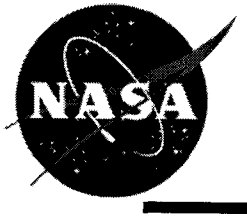
Advanced
Power
Concepts

CISM University Collaboration

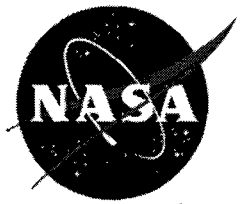


CISM Government Collaboration





System on a Chip Program



Spacecraft Avionics

Spacecraft avionics is a platform providing the resources, both hardware and software, needed to manage a flight mission.

Typical functions supported by avionics systems:

- Guidance and Navigation
  - Spacecraft attitude and orientation
  - Propulsion control
- Articulation and control to support communications and science platforms
- Telecommunications - formatting, encoding/decoding, data buffering
- Power management and distribution
- Event sequencing

Attributes of spacecraft avionics:

- **Support diversity of sensors (avionics, housekeeping and science) with unique interface requirements**
- **Survivability in extreme environments (radiation, high/low temperatures, high g)**
- **Low mass, volume, and power**
- **Long life and reliability**
- Fault tolerance
- Testability-self test (JTAG, BIST)
- Modular and scalable

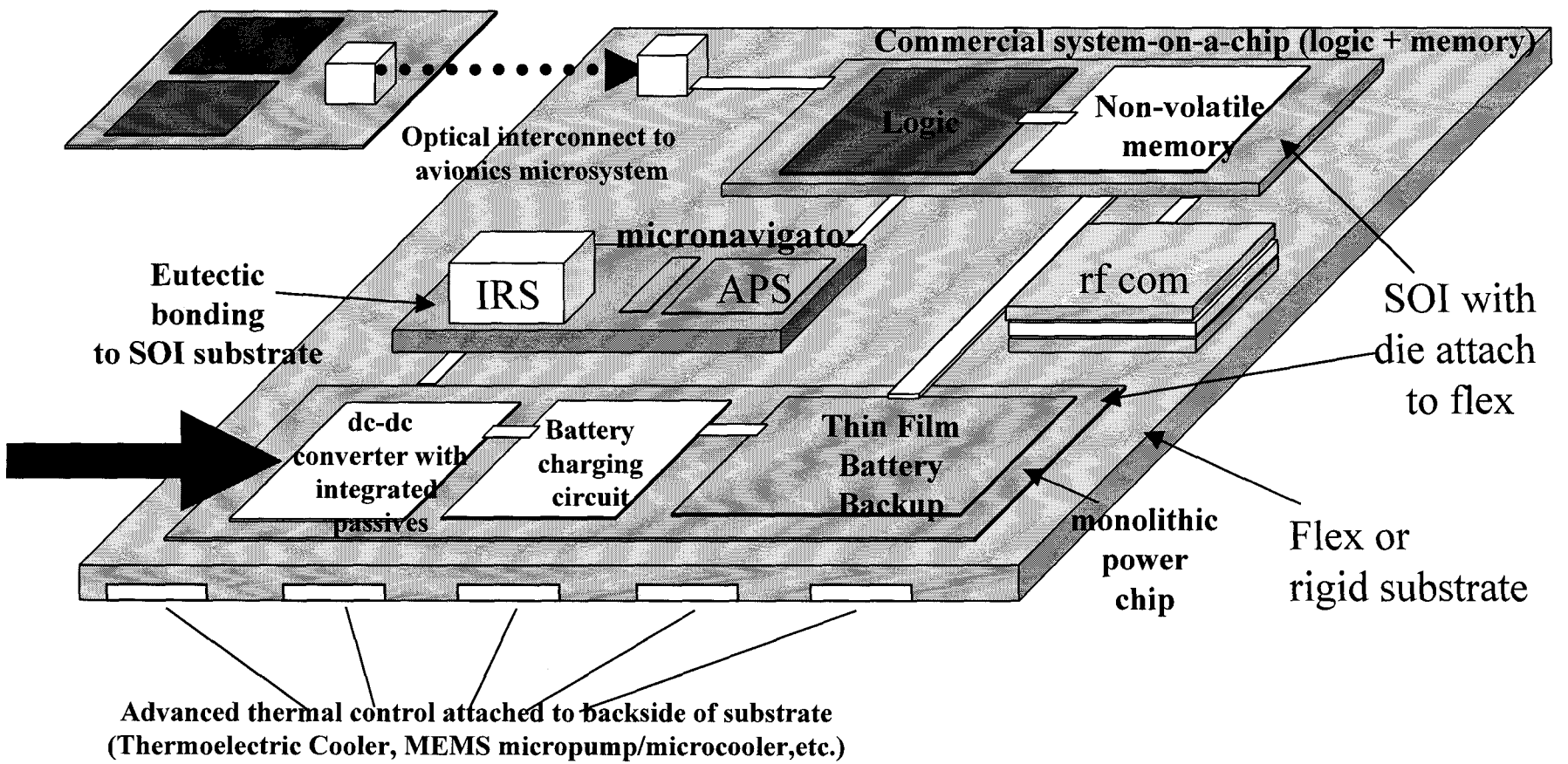
SOAC based system: Example

Example of an
Avionics Microsystem
enabled by SOAC technology

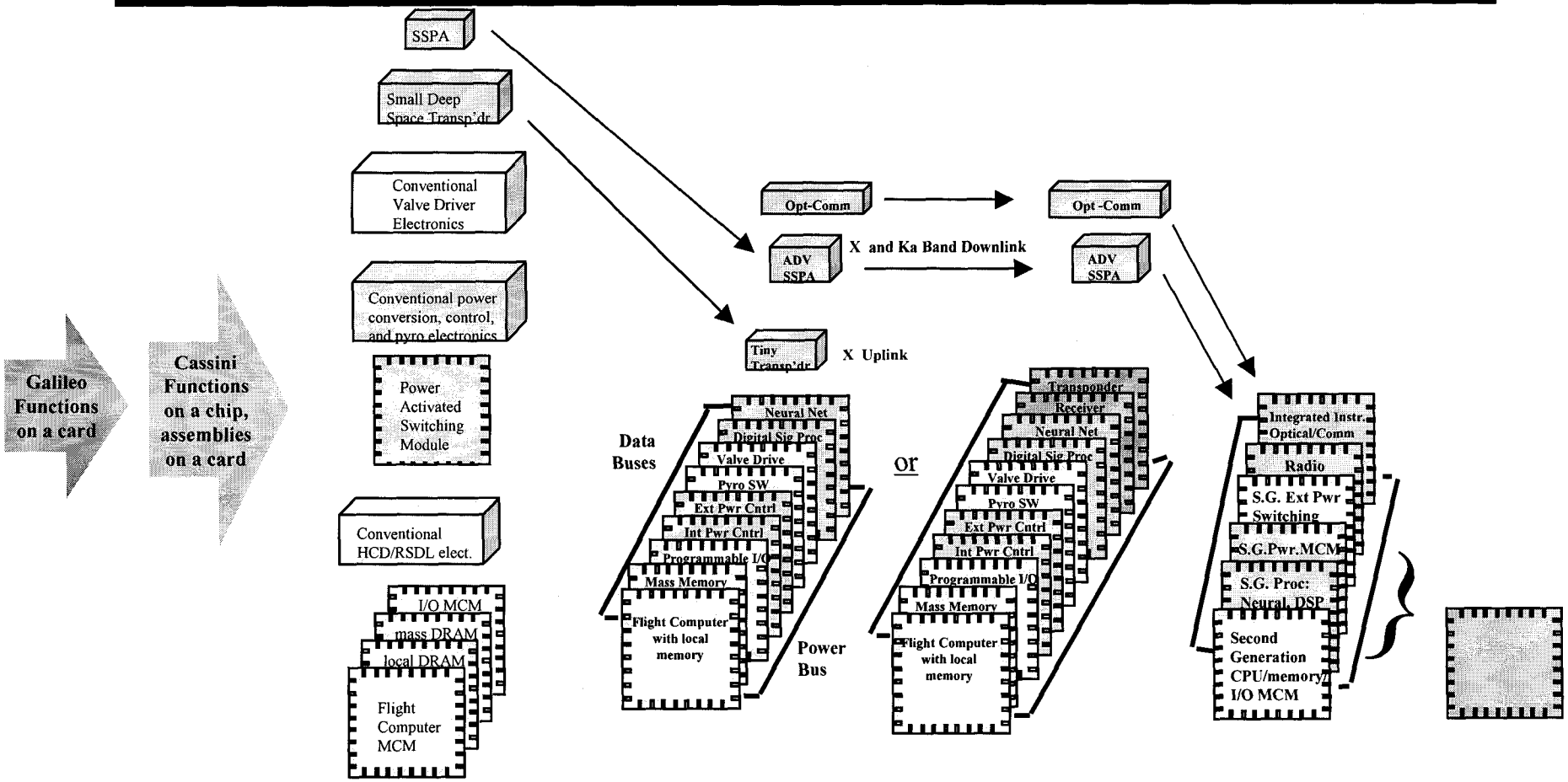
Multiple Science Packages of Distributed Sensors (attached to arm, sail, deployable structure, etc.)

Products are highly adaptable and modular and can be configured to any mission type (sails, rovers, cluster missions) using advanced

die attach, and wafer scale and 3-D packaging

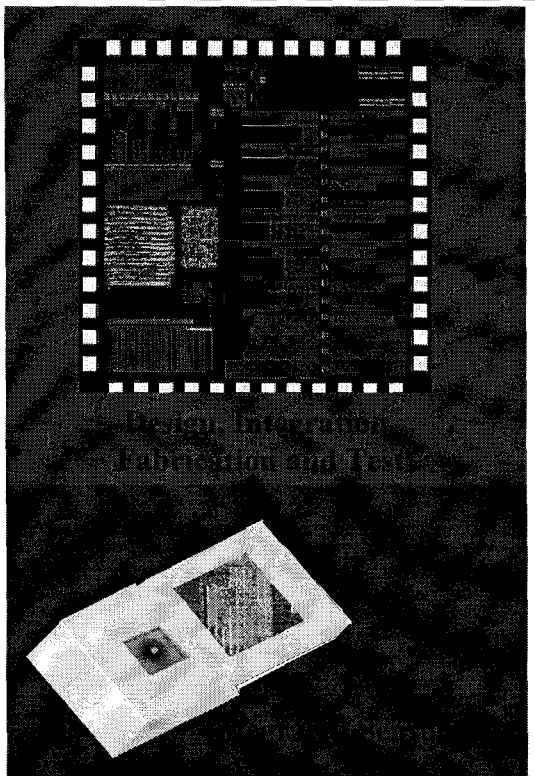


A Conceptual Roadmap: From Boxes to SOAC

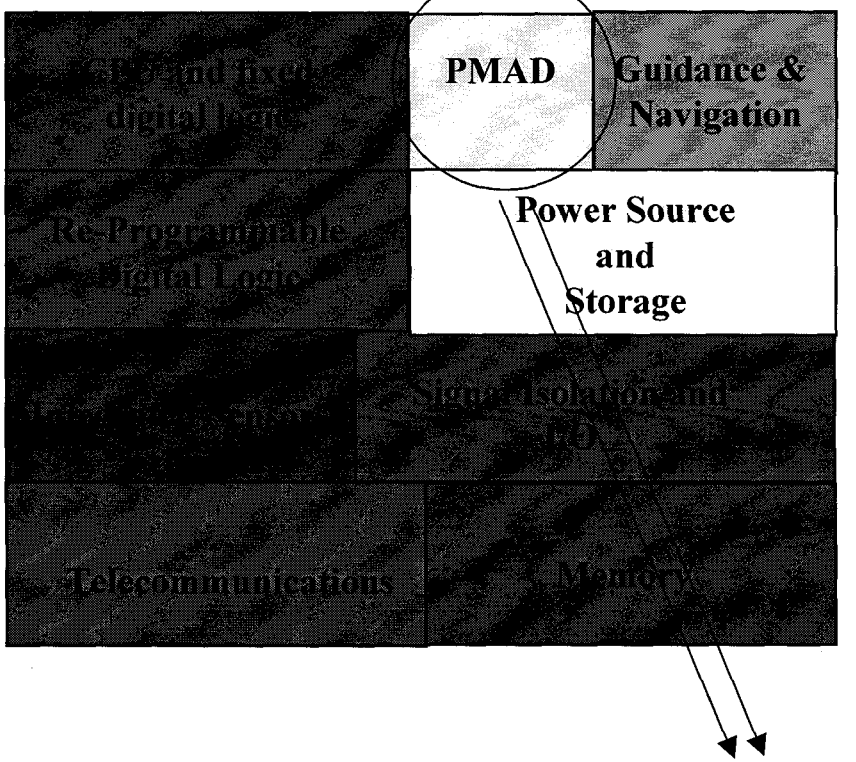


HCD/RSDL = Hardware Command Decoder/Need Solar Downlink **PWR** = Power
MCM = Multi-chip Modes **OPT** = Optical **SSPA** = Solid State Power Amplifier
NMP = New Millennium Program **DS1**= Deep Space 1, 1st NMP Technology Demo Flight

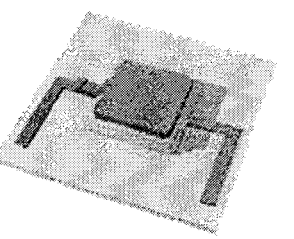
SOAC-Technology



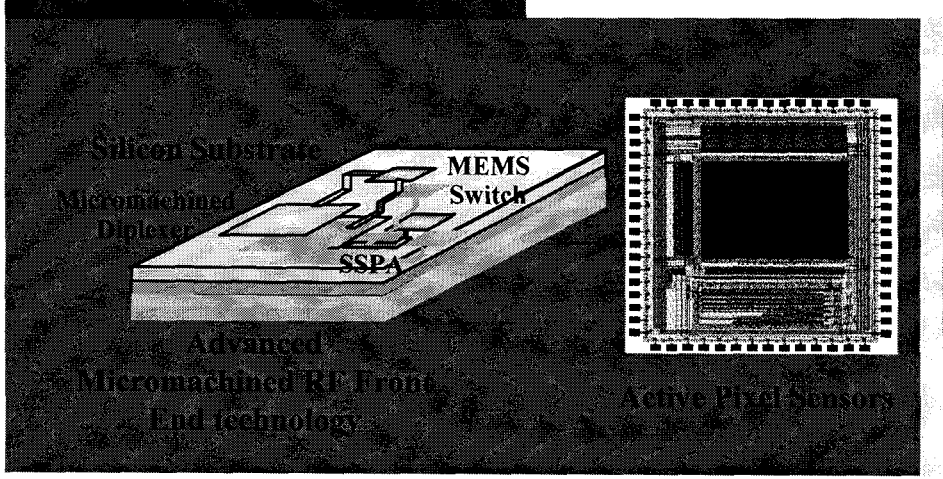
Design, Integration, Fabrication and Testing



Micromechanical Inertial Reference System



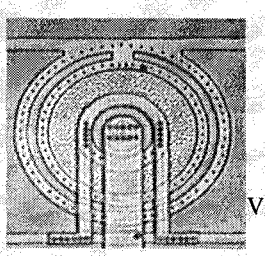
On-Chip Power Source

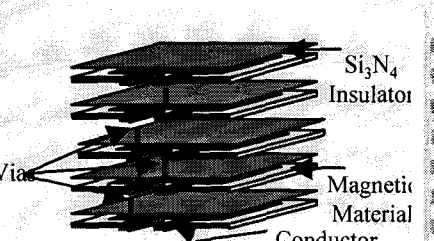


Advanced Micromachined RF Front-End Technology

Active Pixel Sensors

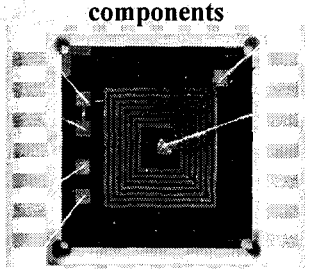
PMAD





Thin film microtransformers

Embedded passive components

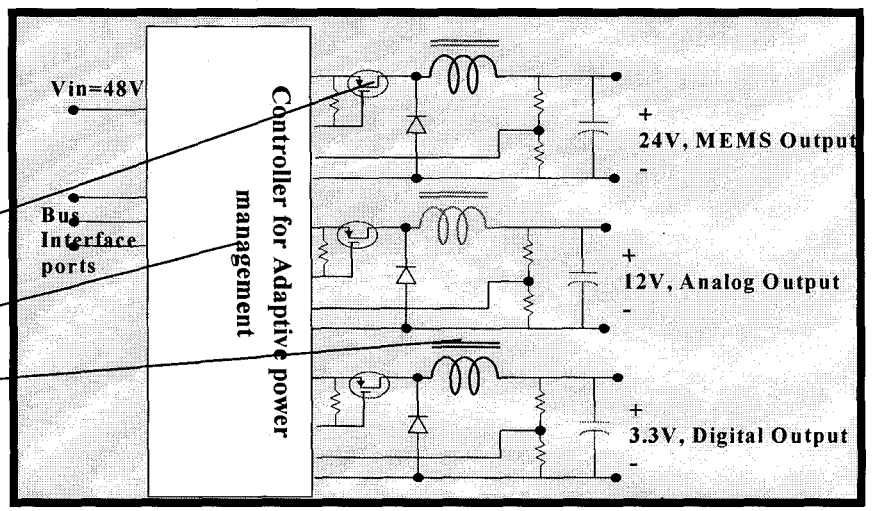


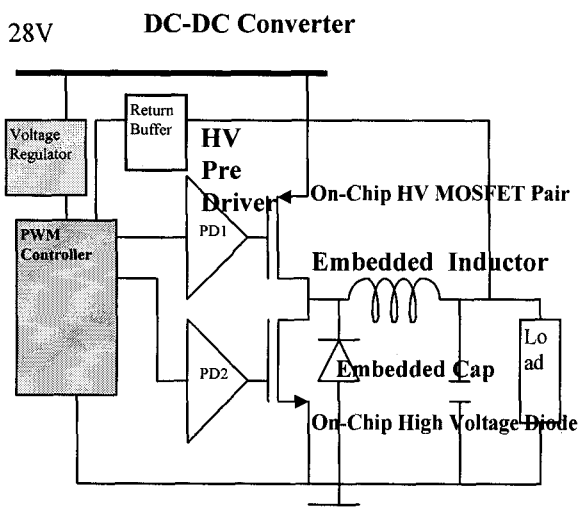
An Integrated Output Power Supply

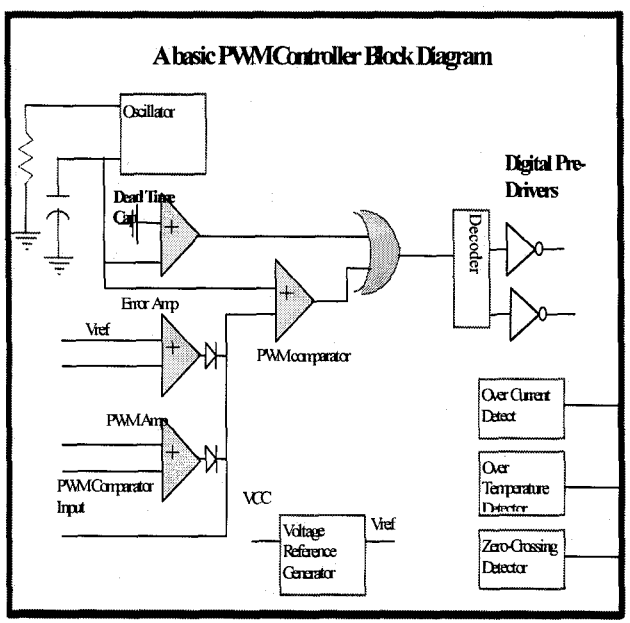
Description:
A high power high efficiency on chip multi output DC-DC power converter with bus interface and adaptive control

Needed Technologies

- **High Voltage Devices in Sub-micron SOI CMOS**
- **Mixed Signal Sub-micron SOI Power Circuit Library**
- **Embedded Passives**

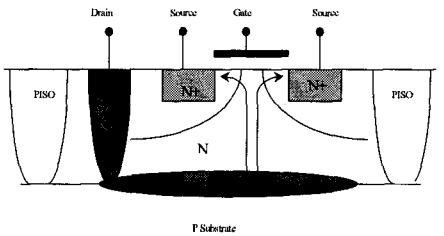






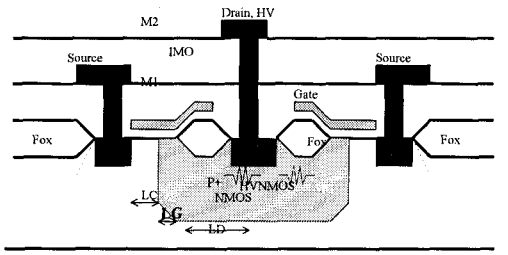
Cell Type	
Low Voltage	Precision References
Low Voltage	High-Speed Differential Input Amplifiers
Low Voltage	Comparators
Low Voltage	Operational Amplifiers
Low Voltage	Analog Buffers
Low Voltage	Oscillators
Low Voltage	Phase/Frequency Detectors
High Voltage	Rectifiers
High Voltage	Switching Inductor Drivers
High Voltage	Voltage Regulator
High Voltage	Analog Level Translator
High Voltage	Zero Crossing Detector
High Voltage	High Side Gate Pre-Driver

A Rad-Hard SOI CMOS High Voltage Technology



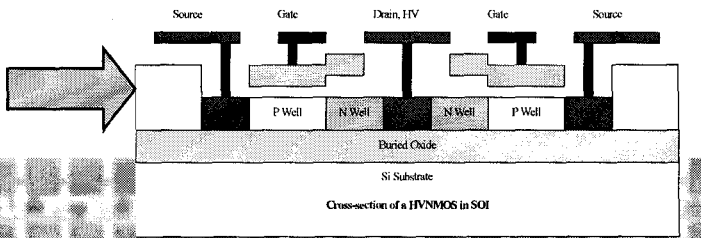
Cross Section of a DMOS in a Power CMOS process

HV Transistors in Power MOS Process



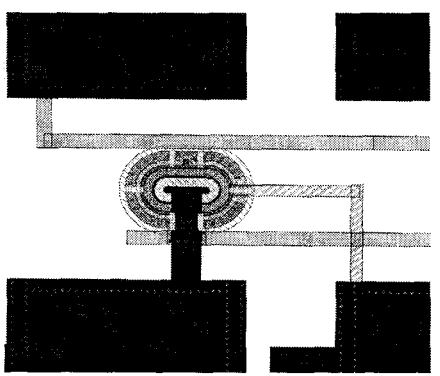
Cross-section of a HV NMOS in sub-micron VLSI bulk CMOS process

HV Transistors Compatible with VLSI CMOS Process

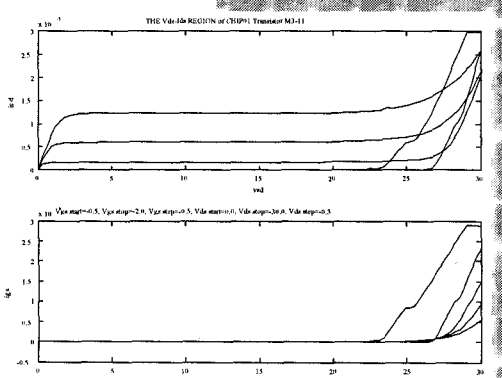


Cross-section of a HVNMOS in SOI

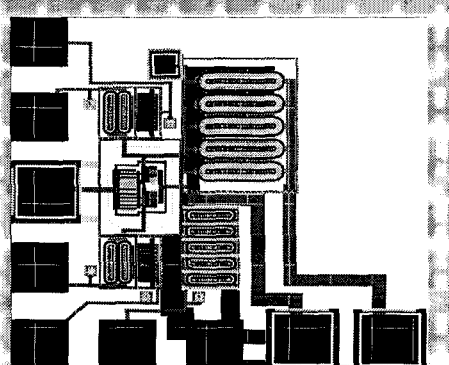
HV Transistors Compatible with SOI CMOS Process



Layout of a HV Transistors in SOI CMOS



Performance of the HV NMOS transistor

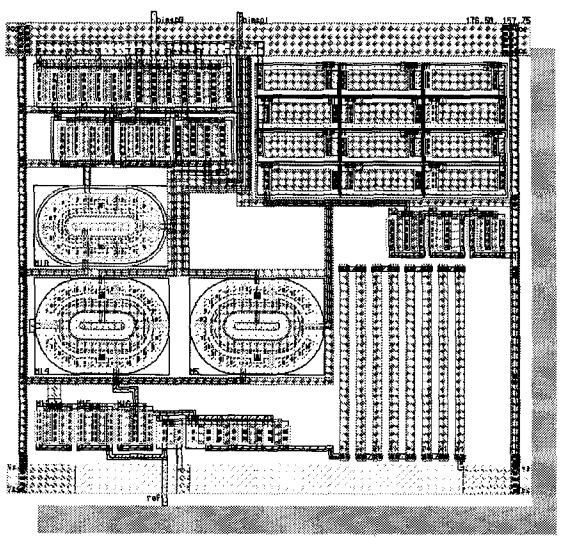


30V Switching HV Driver Circuit

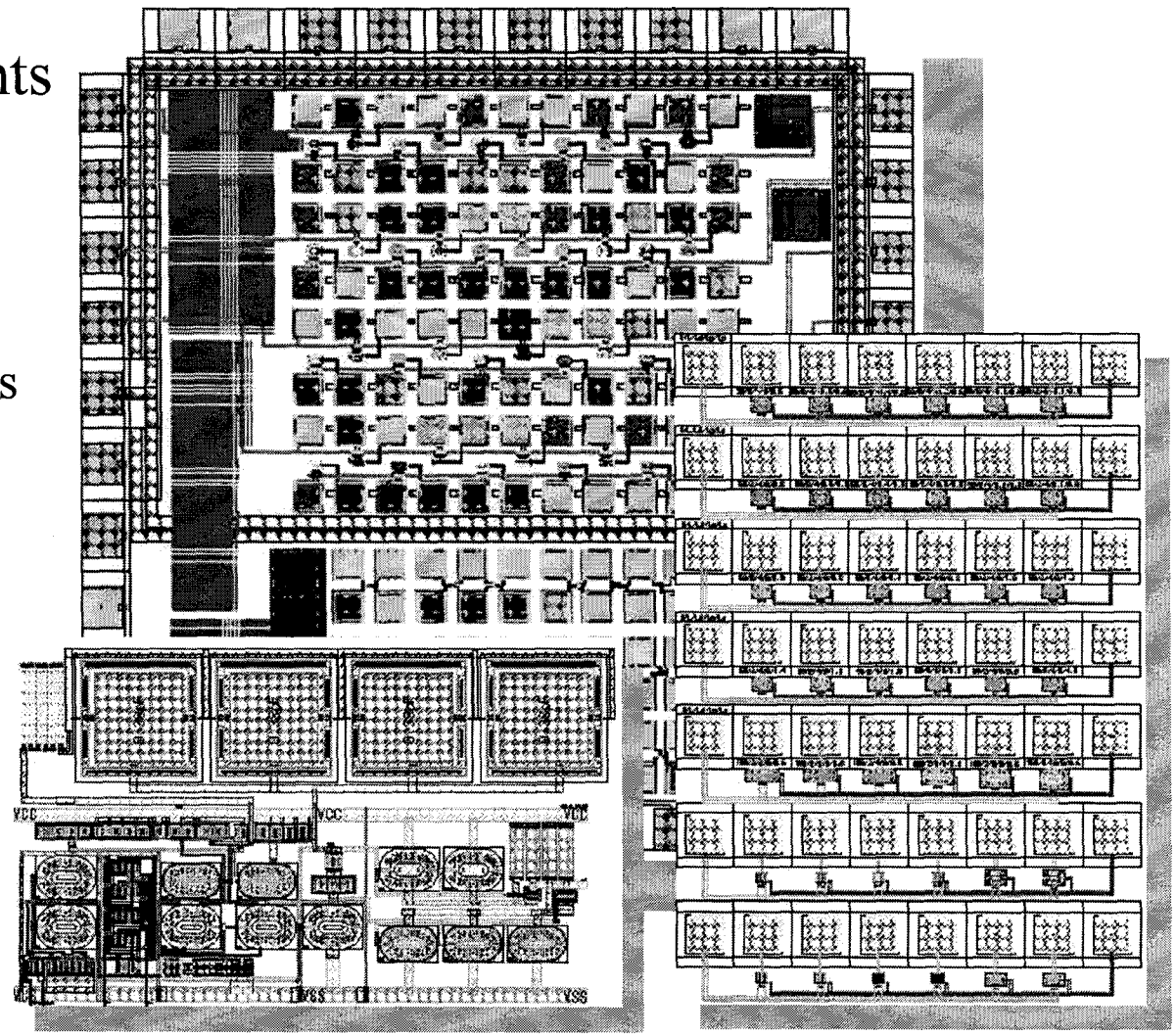
SOI CMOS High Voltage Library

Test Chip Components

- Transistor Arrays
- Current Mirrors
- Biasing Circuits
- Reference Circuits
- Op-Amps



Beta-multiplier layout



High Voltage OpAmp Layout

High Voltage Transistor Test Array

SOI CMOS High Voltage Primitives

Target Performance vs State of the Art:

	EO	Tech. Product
• Resolution	0.8 u	0.35 u
• Rad Hardness	> 1 Mrad	> 1 Mrad
• Voltage Rating	28V	28V

Benefits

A library of high voltage cells in Honeywell's 0.8 um and 0.35 um SOIC technology. Enables higher level of integration of mixed signal components into next-generation ASICs at JPL.

Current Technology Status

Current TRL Level =2

- Started design of the first generation Cells in 0.35u SOIC
- Completed fabrication of 12 chips on 0.8u SOI CMOS line.

Research and Development Team

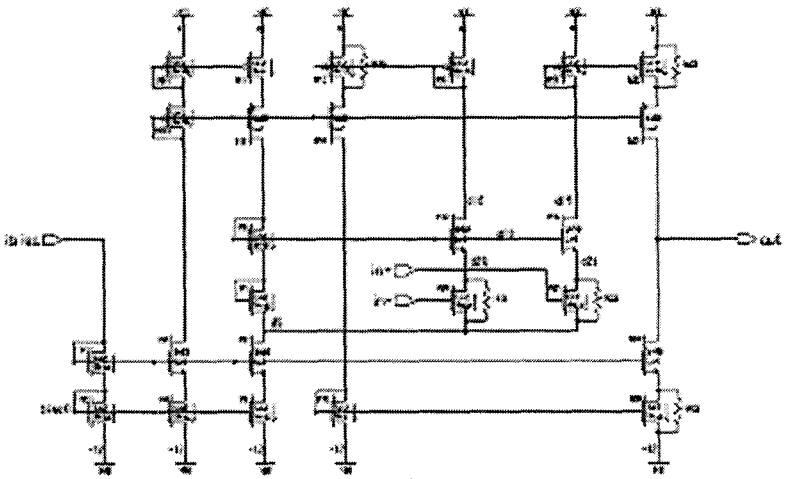
- JPL SOAC
- University of Idaho
- Boeing

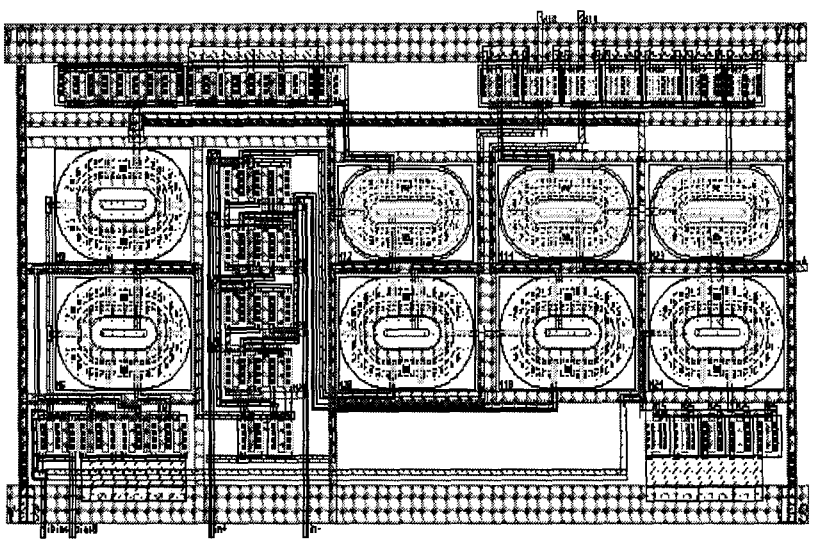
Research Issues:

- Mismatch between transistors
- Power V.S. area
- Substrate effects
- Frequency response

List of circuits in the library

- Differential Amplifiers
- Current Mirrors
- Biasing Circuits
- Bandgap Reference
- OTA
- Op-Amp

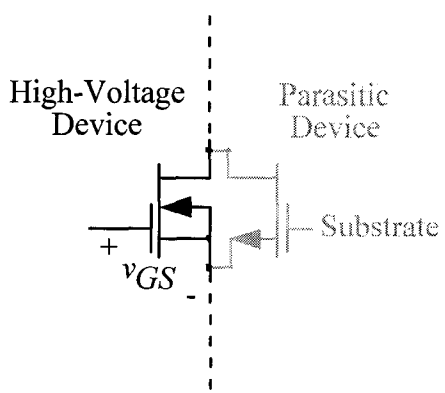


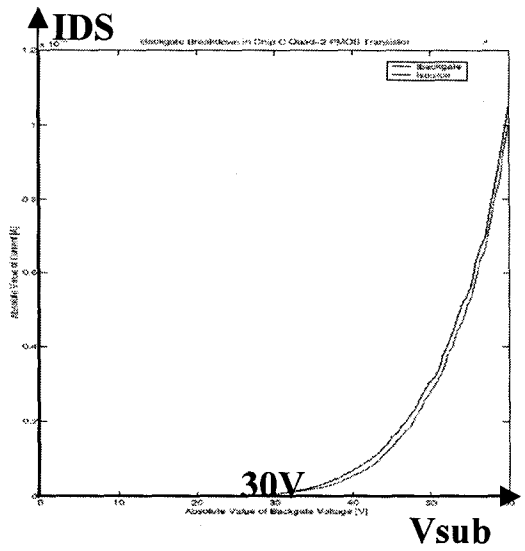


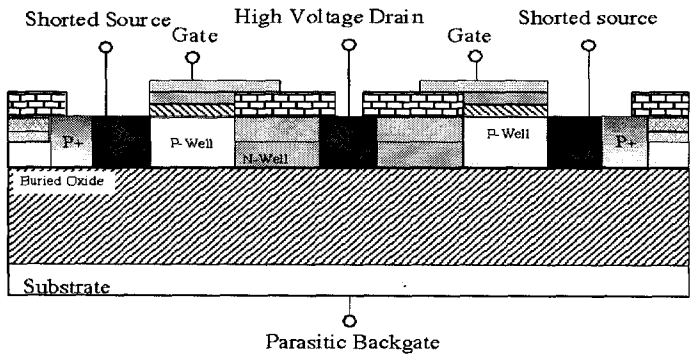
High Voltage OTA schematic and layout

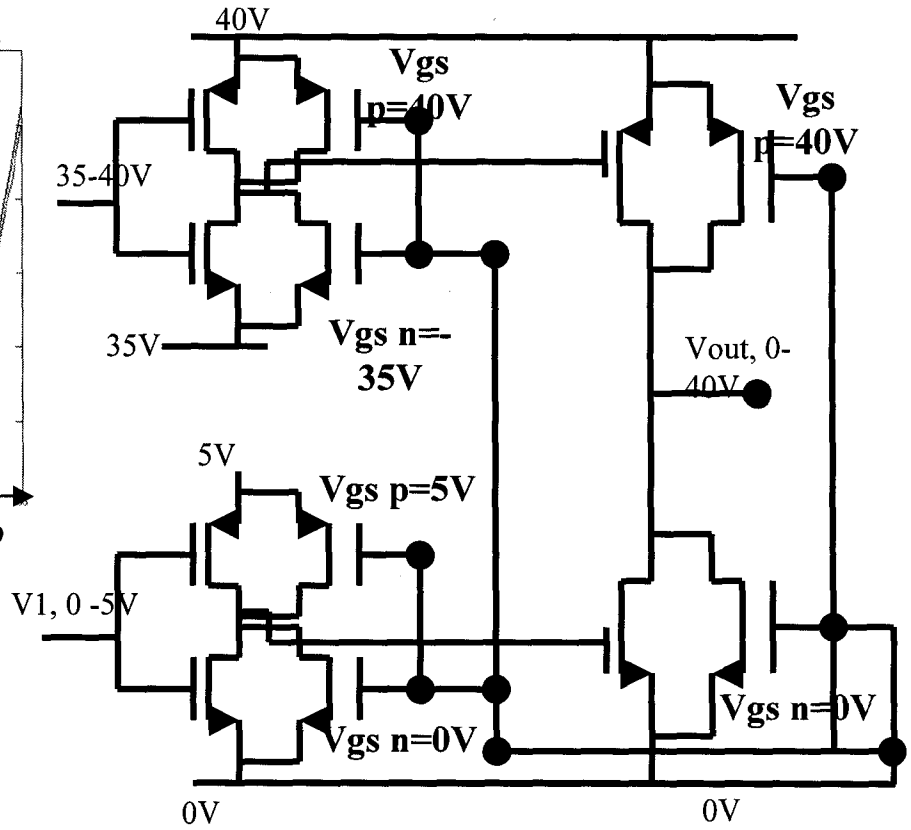
Technical Challenges

- Back Channel Modulation Effects









0.35 um SOI CMOS Adaptive on Chip Back Gate Driver for 60V Operation In Extreme Radiation

Target Performance vs State of the Art:

	EO	Tech. Product
• Performance	0.8 u	0.35 u
• Rad Hardness	≥ 1 Mrad	≥ 1 Mrad

Benefits

- Provides automatic detection of performance degeneration of the circuits due to radiation. Adaptively biases the substrate to compensate for degradations and guarantees operation of the circuit elements up to 60V. Enables total on-chip integration of space-rated Rad Hard power systems with mixed voltage requirements and sensors requiring high voltage requirements in Honeywell's 0.35um SOIC process.

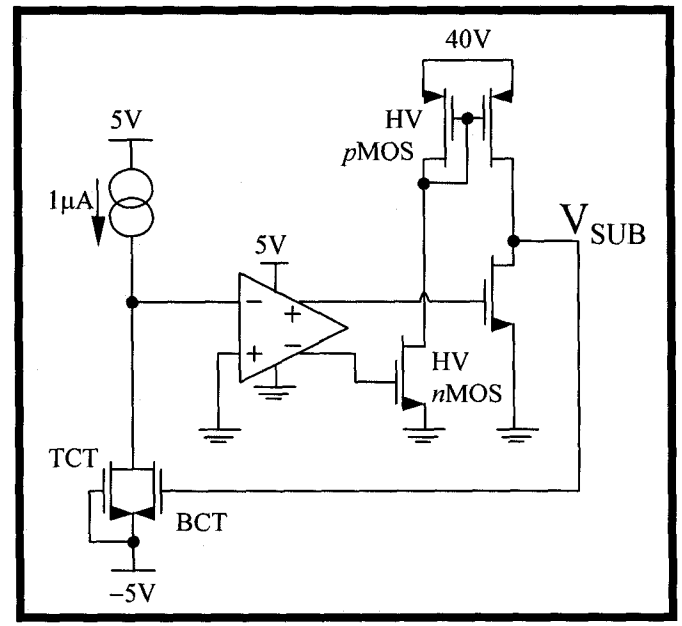
Current Technology Status

Current TRL Level=1+

- Completed fabrication of first version of the device in Honeywell 0.8u SOI CMOS.
- Started the design evaluation and mapping to 0.35u SOI CMOS

Research and Development Team:

- JPL SOAC
- Mississippi State University



Simplified Circuit Diagram for the Back Gate Driver IP

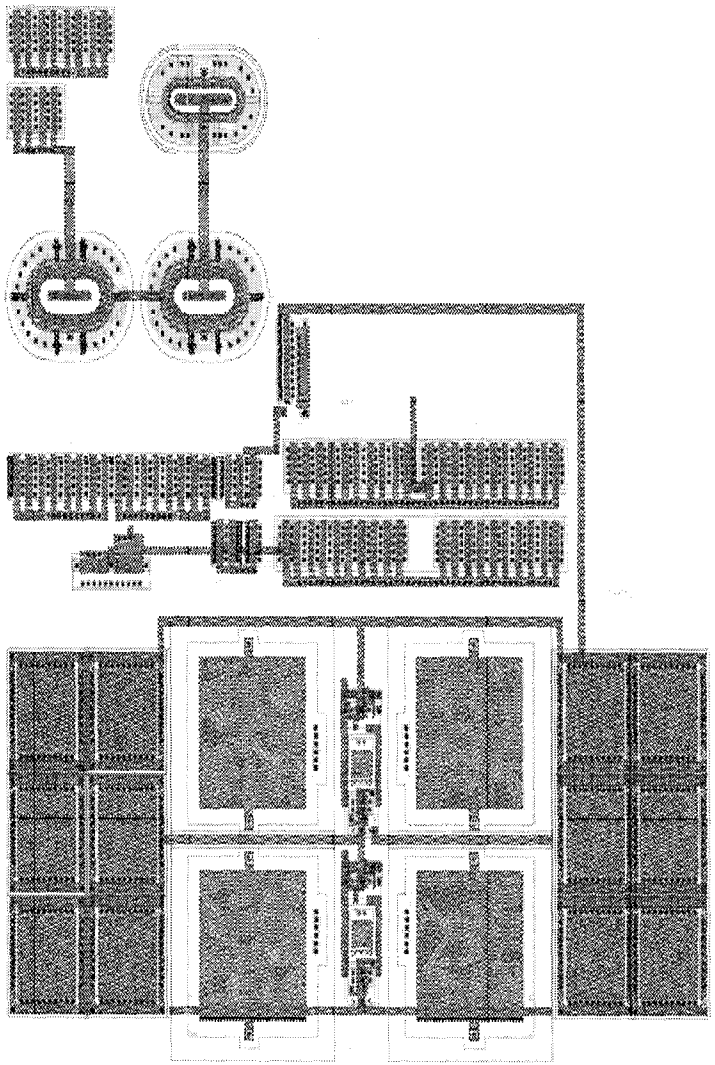
Principles of Operation

- Determine the turn on voltage of the BCT using on chip charge pump
- Bias the substrate using feedback loop

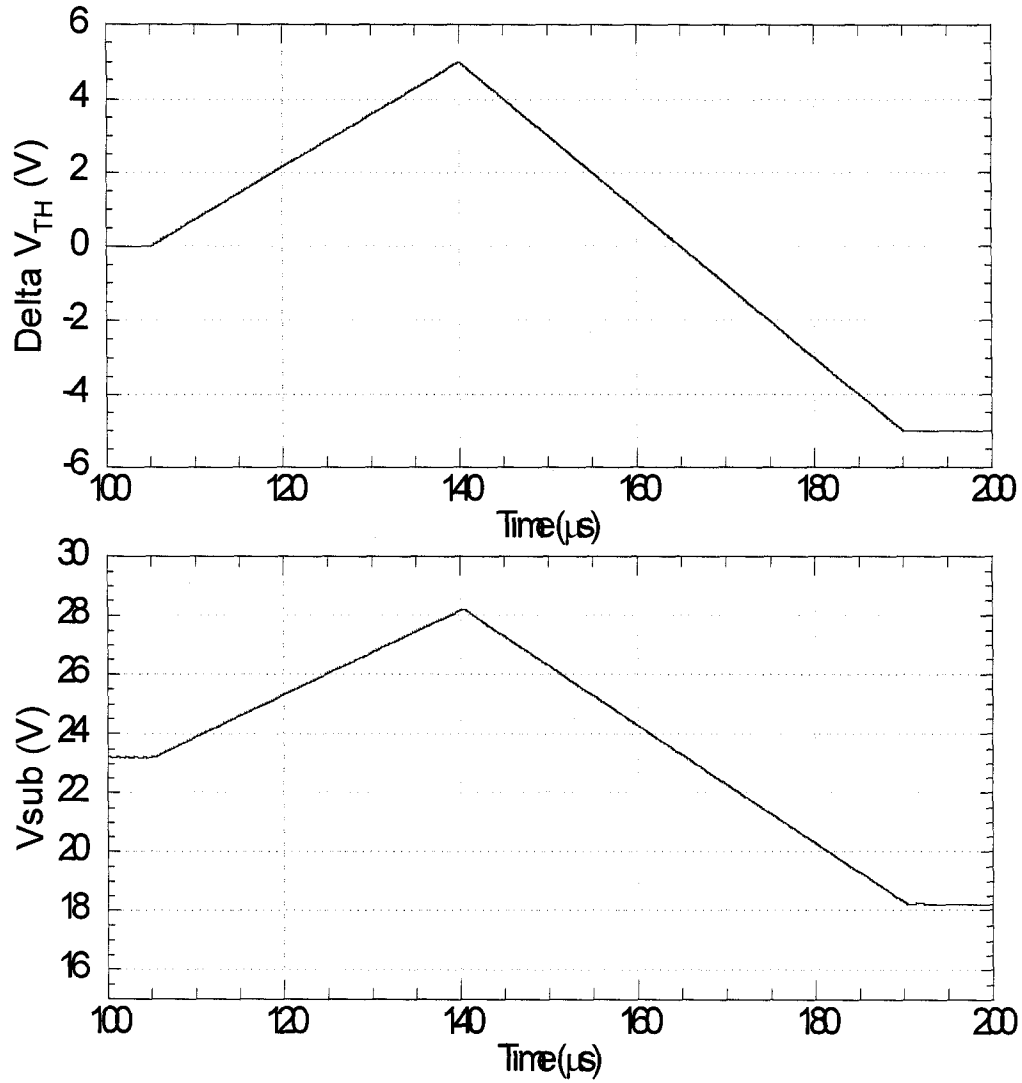
Research Issues

- Support electronics
- Radiation Characteristics

Back Gate Threshold Voltage Tracking



Back Gate Driver Layout



Simulation Results

SOI CMOS Mixed Signal Library

Target Performance vs State of the Art:

	EO	Tech. Product
• Resolution	0.8 u	0.35 u
• Rad Hardness	> 1 Mrad	> 1 Mrad

Benefits

A library of mixed signal cells in Honeywell's 0.35 u SOIC technology. Enables higher level of integration of mixed signal components into next-generation ASICs at JPL. Will eliminate technology obsolescence and enable complete integration of electronics in the RF, Power and other S/C Subsystems.

Current Technology Status

Current TRL Level =2

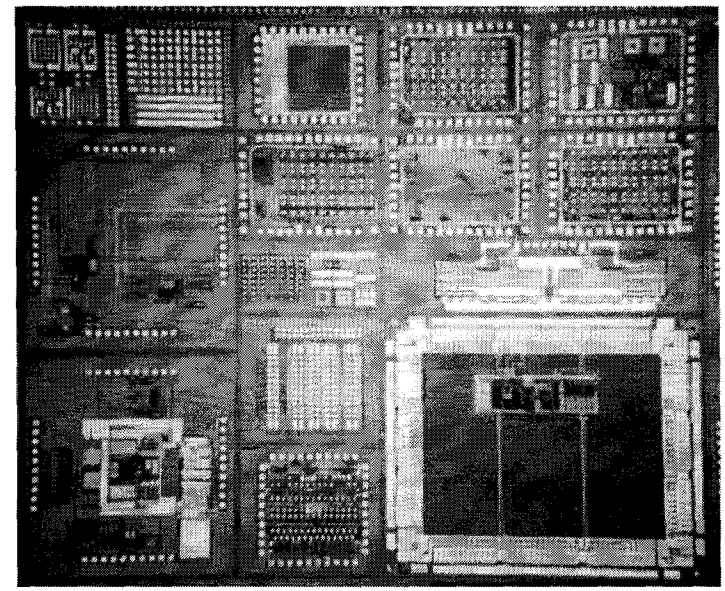
- Started design of the first generation Cells in 0.35u SOIC
- Completed fabrication of 12 chips on 0.8u SOI CMOS line.

Research and Development Team

- JPL SOAC
- Mississippi State University
- University of Idaho
- Boeing

Research Issues:

- Thermal mismatch
- Self-heating
- High body resistance
- Substrate effects

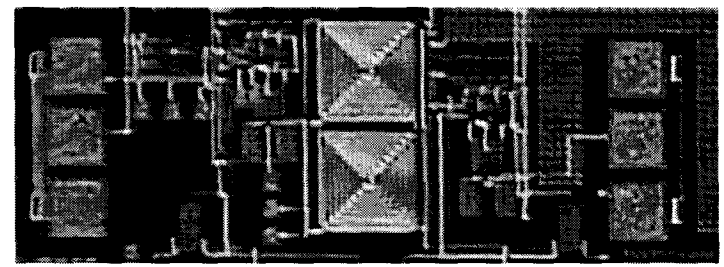


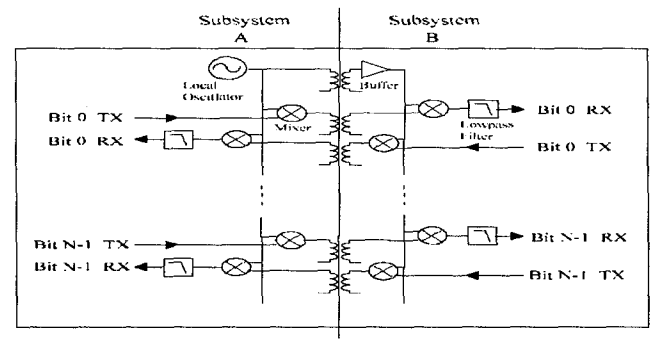
Supply V	Type of circuit	2001 Q1 0.35µm SOIC submission
3.3V	Building Block	High-speed comparator
3.3V	Building Block	Low-power comparator
3.3V	Building Block	Class-AB op amps
3.3V	Building Block	Bandgap voltage reference
3.3V	Building Block	Beta-multiplier current reference
3.3V	Primitive	Single-poly EEPROM devices
3.3V	Primitive	Programmable current reference
3.3V	Primitive	Programmable voltage reference
3.3V	Building Block	Voltage-controlled oscillator
3.3V	Building Block	Active Substrate Driver
3.3V	Complex Cell	VCO-based ADC with SRAM lookup table
3.3V	Complex Cell	Current-mode algorithm ADC
3.3V	Complex Cell	Digital Phase Lock Loop
3.3V	Complex Cell	Power CrossStrap Circuit
3.3V	Complex Cell	Auto Zero Amplifier
3.3V	Building Block	Gilbert Multiplier

Completely Integrated Rad Hard High Speed Multi Channel Signal and Bus Isolation

Target Performance vs State of the Art:

	EO	Tech. Product
•Device type	Discrete	Integrated 0.35 u
•Rad Hardness	> 1 Mrad	> 1 Mrad
•Isolation rating	±40	±20
•Delay	10 ns	1 ns
•Power	10 mA/bit	1 mA/bit
•Mass	<10g	<1g





Benefits

On chip, rad hard, low power multi channel isolation for *high speed 1394 serial bus* using integrated on chip transformers. Can eliminate the present EO data isolation circuits made of discrete components

Current Technology Status

Current TRL Level is 1+

•1st generation proof of concept devices fabricated in Honeywell 0.8u SOI and is being characterized.

•2nd generation design and mapping to Honeywell 0.35u SOI and Peregrine SOS is underway.

Research and Development Team:

- JPL SOAC
- Kansas State University

Principles of Operation

- Digital signals modulated at 1 to 2 GHz
- Totally integrated transformers are used to transmit signals
- Digital signal is demodulated at 2ndary side

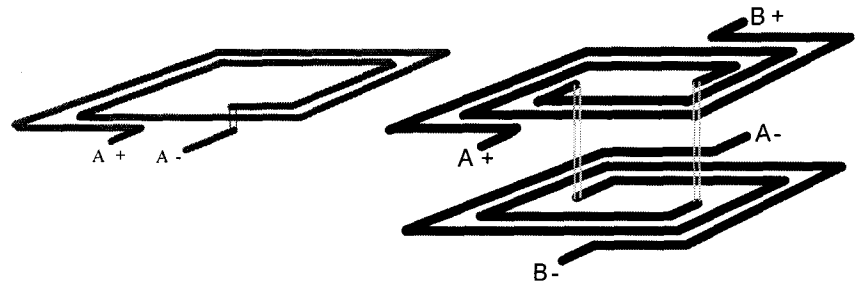
Research Issues

- Minimizing power consumption / area
- Maximizing breakdown (primary-sec)
- SOI vs SOS technology tradeoffs
- On-chip inductor and transformer design

Spiral Inductor/Transformer Modeling and Library Development

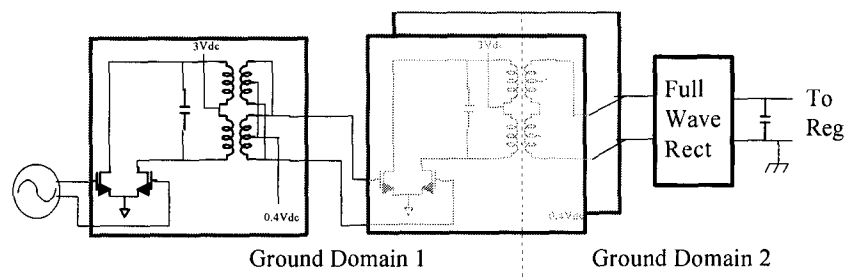
State of the Art in Spiral Inductors/Transformers

• Useful values	1 nH to 500 nH
• Frequency of operation	100 MHz to 20 GHz
• Quality factors	3 to 10+
• Transformer coupling	> 0.8



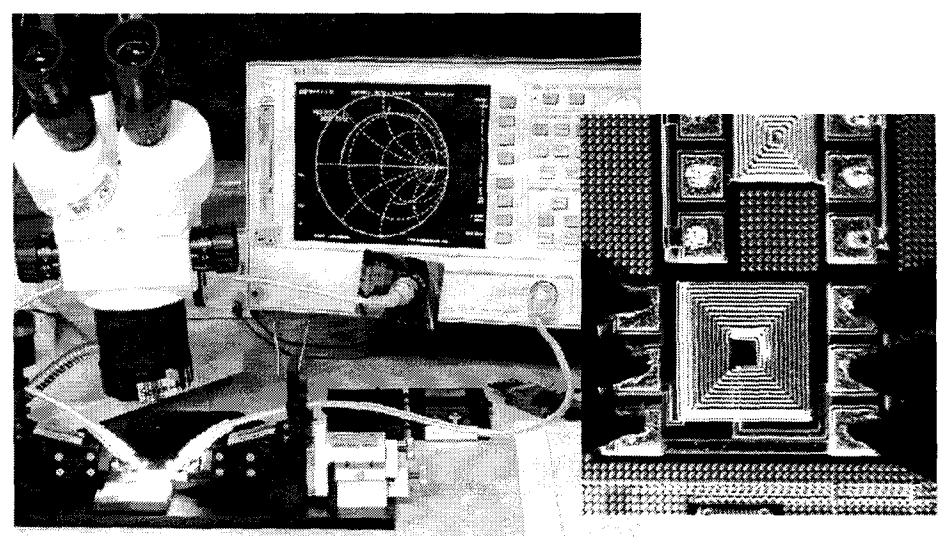
Applications

- On-chip power/ground isolation
- Low-power, fully-integrated, comm systems
- Integrated power supplies
- Significant reductions in size/weight over discrete designs



Library Development

- Array of 36 inductors/transformers in Honeywell 0.35 SOI
- 120um to 480um outer dimensions
- Optimized performance (ground shields, via-stacks,..)
- Full 2-port S-Parameter characterizations



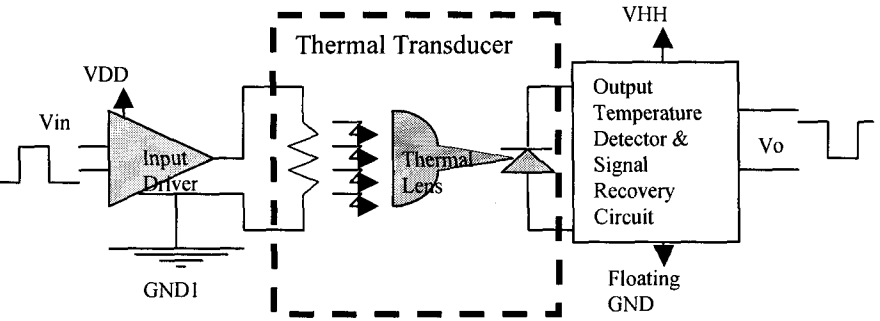
Research and Development Team:

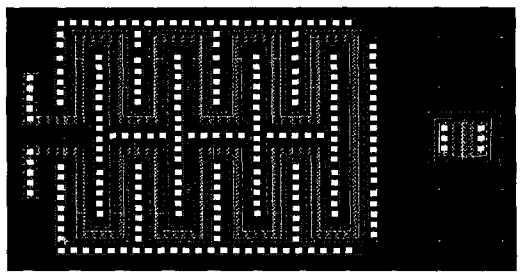
- JPL SOAC
- Kansas State University

Completely Integrated Rad Hard Medium Speed Thermally Coupled Multi Channel Signal and Bus Isolation

Target Performance vs State of the Art:

	EO	Thermal Xdcr
• Device type	Discrete	Integrated 0.35 u
• Rad Hardness	> 1 Mrad	> 1 Mrad
• Isolation rating	±40	±20
• Mass	<10g	<1g
• On-chip recovery	no	yes





Benefits

On chip low power rad hard multi channel isolation for medium speed I2C serial bus uses thermal transducers. Can eliminate the present EO data isolation circuits made of discrete components.

Current Technology Status

Current TRL Level is 1

- Initial proof of concept devices fabricated in Honeywell 0.8u SOIC and are being characterized.
- 2nd pass design concepts and mapping to Honeywell 0.35u SOIC is underway.

Research and Development Team

- JPL SOAC
- University of Arkansas (Prof. Alan Mantooth, Ty McNutt, Seth Henry)
- Mississippi State (Prof. Ben Blalock)

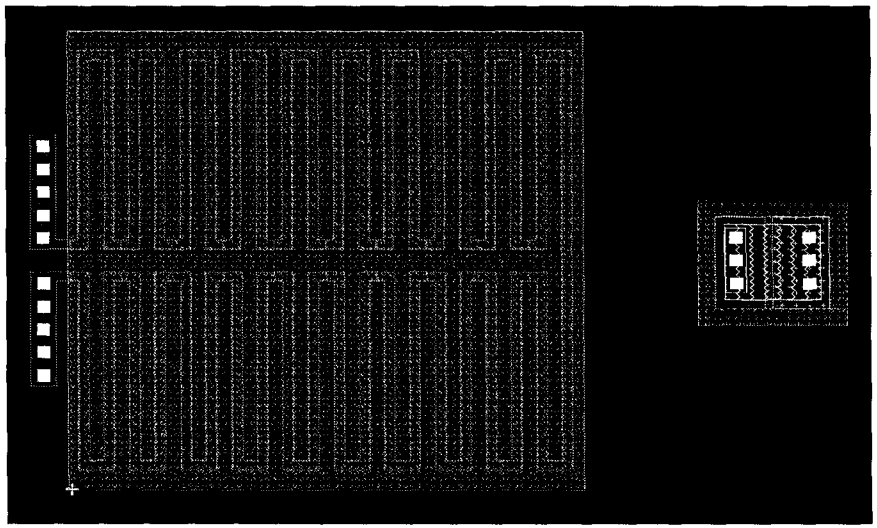
Principles of Operation

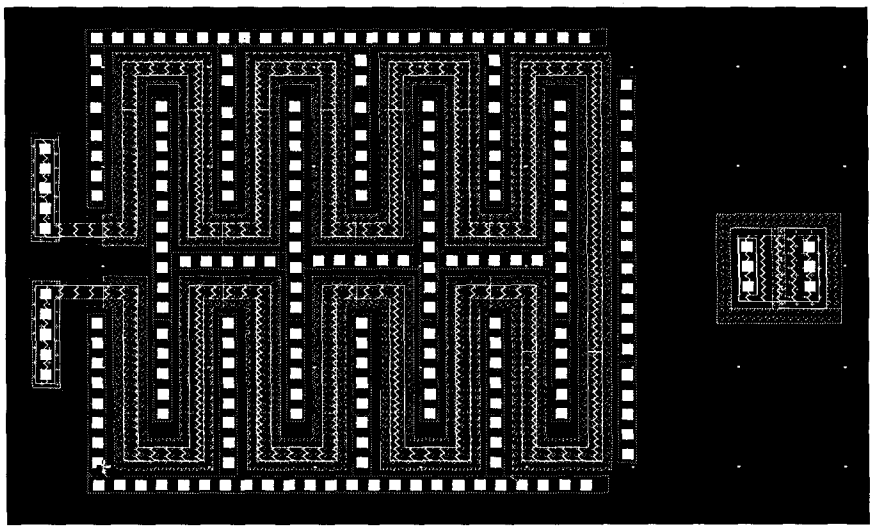
- Digital signal is converted to heat
- Heat propagates through Si02 layer to Al and ultimately to diode
- Diode current bias changes
- Digital signal is reconstructed

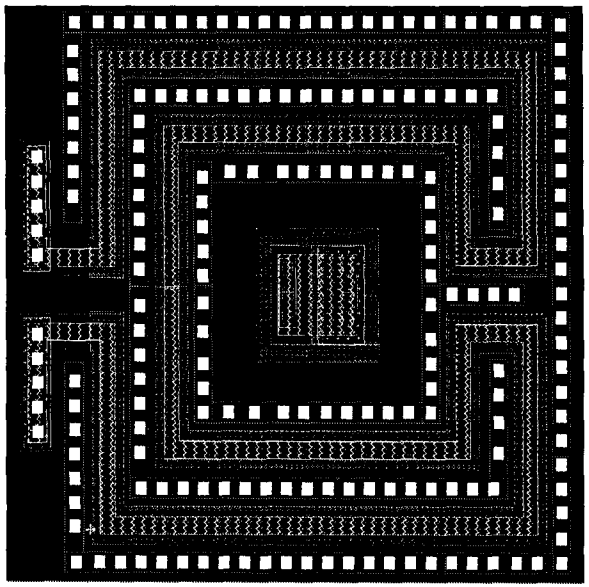
Research Issues

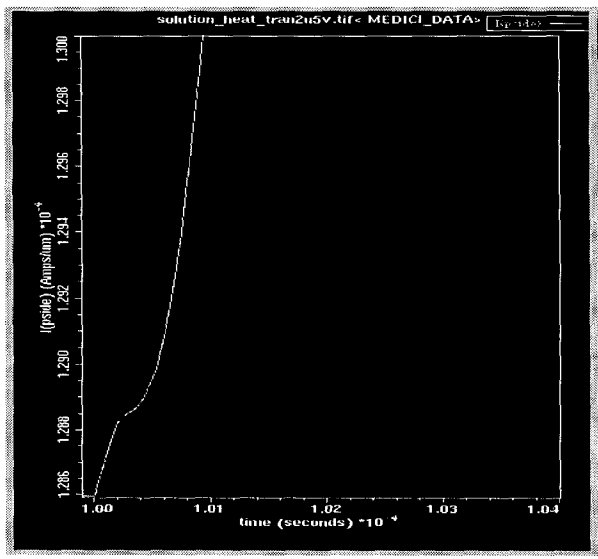
- Propagation delay
- Power dissipation levels
- Efficiency of conversion
- Achievable electrical isolation
- Geometrical configuration

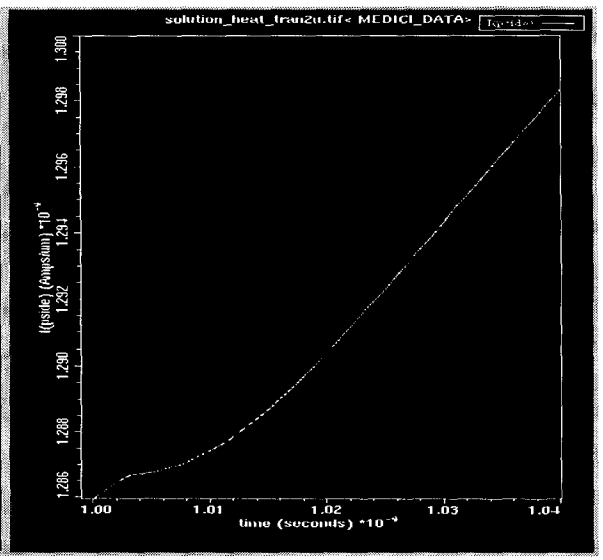
0.8 μm Layouts and 2-D Simulation Results

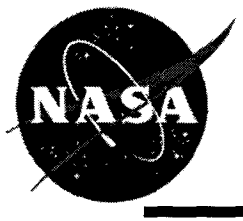




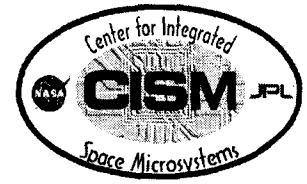




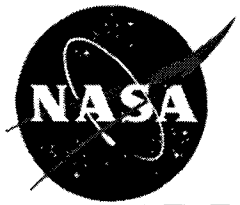




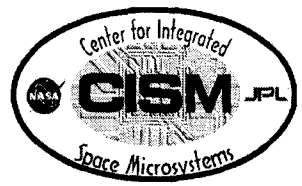
Technical Challenges



- Porting mixed-signal, mixed-voltage designs and related technology to smaller and smaller sub-micron SOI CMOS processes.
- More accurate modeling of high voltage SOI devices including:
  - Thermal mismatch
  - Self-heating
  - High body resistance
  - Substrate effects
- Mixed-signal system noise issues.
- Mapping algorithms between SOI CMOS and bulk CMOS for mixed-voltage analog applications.



Summary



- CISM, a JPL Center of Excellence, is an element of NASA's Deep Space Systems Development Program.

- CISM/SOAC program, focuses on the integrated circuit technology that are specific to NASA's deep space needs and not addressed by commercial companies

- Unique to avionics for deep space are needs for diverse mixed signal sensor interfaces and survivability in extreme environment (radiation resistance….)